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In re PATENT application of	)
Minoru MIYAZAKI et al.	) Group of Art Unit: 2825
Serial No. 10/620,420	) Examiner: Calvin Lee
Filed: July 17, 2003	)
For: ELECTRONIC CIRCUIT	)

VERIFICATION OF TRANSLATION

Commissioner for Patents
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Sir:

I, Kazuya Morikawa, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, declare:

that I am well acquainted with both the Japanese and English languages; and

that to best of my knowledge and belief the following is a true and correct translation of Japanese Patent Application Serial No. 5-23289 filed on January 18, 1993.

I further declare that all statements made herein of my own knowledge are true and that all statements are made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 21th day of July, 2004

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[Title of the Invention] ELECTRONIC CIRCUIT

[Number of Claims] 7

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[Claiming Priority based on Prior Application]

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[List of Attachment]

[Attachment]	Specification	1
[Attachment]	Drawing	1
[Attachment]	Abstract	1

[Name of Document] Specification

[Title of the Invention] ELECTRONIC CIRCUIT

[Scope of Claim]

[Claim 1] An electronic circuit comprising wirings characterized by comprising:

a first layer mainly including titanium and nitrogen in contact with a semiconductor film mainly including silicon with a thickness of 1500 Å or less; and

a second layer mainly including aluminum provided so as to be in contact with the first layer.

[Claim 2] The electronic circuit of claim 1 is characterized in that the semiconductor film mainly including silicon has a N- or P-type conductivity.

[Claim 3] The electronic circuit of claim 1 is characterized in that the semiconductor film mainly including silicon has a thickness between 100 Å or more and 750 Å or less.

[Claim 4] The electronic circuit of claim 1 is characterized in that a film mainly including silicon oxide in which a same impurity as the one doped into the semiconductor film is included is under and in intimate contact with the semiconductor film mainly including silicon.

[Claim 5] The electronic circuit according to claim 1, the first layer 1 is in contact with a conductive oxide thin film.

[Claim 6] An electronic circuit comprising wirings characterized by comprising:

a first layer mainly including titanium in contact with a semiconductor film mainly including silicon with a thickness of 1500 Å or less;

a second layer mainly including titanium and nitrogen provided so as to be in contact with the first layer; and

a third layer mainly including aluminum provided so as to be in contact with the second layer.

[Claim 7] An electronic circuit comprising wirings characterized by comprising:

a first layer mainly including titanium and nitrogen in contact with a semiconductor film mainly including silicon with a thickness of 1500 Å or less;

a second layer mainly including titanium and nitrogen provided so as to be in

contact with the first layer; and

a third layer mainly including aluminum provided so as to be in contact with the second layer, wherein

a ratio of titanium to nitrogen of the first layer is larger than that of the second layer.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention]

The present invention relates to an electronic circuit which is formed over an insulating substrate; which has a semiconductor layer of thin silicon and the like such as a thin film transistor; and which is required to connect the semiconductor layer and wirings.

[0002]

[Prior Art]

Until now, in a thin-film devices such as a thin film type insulated-gate field-effect transistor (TFT), a thin semiconductor film such as silicon used as an active layer has about 1500 Å thick. Therefore, when an electrode is to be formed over the thin semiconductor film, adequate contact can be made by bringing a metal such as aluminum into direct and intimate contact with the film, as is the case with prior art IC fabrication techniques. A silicide such as aluminum silicide is usually formed by a chemical reaction between the aluminum and the semiconductor-component such as silicon in this kind of contact portion; however there are no problems since the semiconductor layer is sufficiently thicker than the silicide layer.

[0003]

[Problem to be solved by the Invention]

However, researches conducted recently have demonstrated that the characteristics of the TFTs is improved when the thickness of the active layer is decreased up to 1500 Å or less, for example, between about 100 Å to 750 Å. However in the case of forming an electrode over such a thin semiconductor film (active layer), it has not been possible to make good contact by the prior art techniques since the thickness of the silicide layer grows almost up to the thickness of the semiconductor layer, thus severely deteriorating the

electrical characteristics of the contact. When a stress such as a voltage is kept applied to the contact for a long time, the contact deteriorates seriously.

[0004]

In order to improve the characteristics of the TFTs heat treatment within hydrogen ambient having 400 °C or less, for example, 200 °C to 350 °C is required to be performed. However, there is a problem of deteriorating the characteristic of the TFTs in which the thickness of the semiconductor film is 1500 Å or less, since the formation of the silicide is extremely promoted due to the heat treatment.

[0005]

The present invention is proposed in order to solve the above-mentioned problems. And it is an object of the present invention to provide a preferable contact between wirings and a semiconductor layer, which can withstand heat treatment with 300 °C or more, and to improve the reliability.

[0006]

[Means for Solving the Problem]

The present invention relates to an electronic circuit having a semiconductor layer in which silicon with a thickness of 1500 Å or less, preferably 100 Å or more and 750 Å or less is in its main component. For example, the invention is applicable to an electronic circuit having TFTs each provided with an active layer with a thickness of 1500 Å or less. The effects of the present invention become conspicuous as the thickness of the semiconductor layer decreases.

[0007]

One feature of the first structure of the present invention is that the above-described thin semiconductor layer is either in intimate contact with the top surface of the insulating substrate such as glass or formed over the substrate via some insulating film; a first layer including mainly of titanium and nitrogen is partially or totally in intimate contact with the semiconductor layer: a second layer including mainly of aluminum is formed on the top surface of the first layer; and the wirings are formed according to the first and the second layers. The bottom surface of the second layer is substantially totally in intimate contact with the first layer. It is possible to form a third layer including mainly of titanium and

nitrogen over the second layer.

[0008]

One feature of the second structure of the present invention is that the thin semiconductor layer is either in intimate contact with the insulating substrate such as glass or formed over this substrate via some insulating film; a first layer including titanium is partially or totally in intimate contact with the semiconductor layer; a second layer including mainly of titanium and nitrogen is in intimate contact with the top surface of the first layer; a third layer mainly including aluminum is formed on the top surface of the second layer; and the wirings are formed according to the first to the third layers. Of course, other layer may be formed on the third layer.

[0009]

One feature of the third structure of the present invention is that the thin semiconductor layer is either in intimate contact with the insulating substrate such as glass or formed over the substrate via some insulating film; a first layer including both titanium and nitrogen as its main component is partially or totally in intimate contact with the semiconductor layer; a second layer including mainly of titanium and nitrogen is in intimate contact with the top surface of the first layer; a third layer including mainly of aluminum is formed on the top surface of the second layer; and the wiring is formed according to the first to the third layers. Further, one feature of the present invention is that the ratio of the titanium to the nitrogen (titanium/nitrogen) in the first layer is greater than that of the second layer.

[0010]

In any structure of these structures, the portions of the thin semiconductor film with which the first layer is in intimate contact show N- or P-type conductivity. Preferably, the dose in these portions is 1×10^{19} to 1×10^{20} /cm^{-2}. The impurity may be introduced by a well-known ion implantation method or plasma doping. Where such impurity ions are accelerated to a high energy and introduced, the dose is preferably between 0.8×10^{15} and 1×10^{17}/cm^{-2}. Also, laser doping using laser irradiation within ambient of an impurity gas may be utilized. This method is described in Japanese Patent application Ser. No. 283981/1991, filed October 4, 1991, and No. 290719/1991, filed October 8, 1991.

Preferably, the sheet resistance of these portions is preferably 1 kΩ/□ or less.

[0011]

Silicon oxide may be formed while attaching to the lower part of the thin semiconductor. At this time, in the silicon oxide film, an impurity which is the same as the one doped into the thin semiconductor may be included.

[0012]

In the first layer of the above-described first structure, the ratio of the titanium to the nitrogen contained as its main component may differ according to the thickness. Besides titanium and nitrogen, other element such as silicon and oxygen can be contained as its main component. For example, the portion of the first layer which is close to the semiconductor layer may includes mainly of titanium and silicon. The portion of the first layer which is close to the second layer may include mainly of titanium and nitrogen. For instance, the ratio of nitrogen to titanium (nitrogen/titanium) may be set close to a stoichiometric ratio (0.8 or more). In the intermediate region, the component may be made to vary continuously.

[0013]

Generally, a stoichiometric material (titanium nitride) containing nitrogen and titanium has excellent barrier characteristics and prevents diffusion of aluminum and silicon. However, the material shows a high contact resistance with silicon. Therefore, it is not preferable to use such a material directly for formation of contact. On the other hand, astoichiometric material (titanium silicide) containing titanium and silicon (titanium silicon, titanium silicide) exhibits low contact resistance with the semiconductor layer including mainly of silicon. This is advantageous to form ohmic contact. However, aluminum and the like tend to easily diffuse. For example, the aluminum of the second layer diffuses through the first layer, thus forming aluminum silicide in the semiconductor layer.

[0014]

The complex layer structure described above has been formed to solve these problems. In particular, the portion which is in contact with the second layer is made of substantially stoichiometric titanium nitride and hence the titanium nitride has excellent barrier characteristics. This prevents the aluminum of the second layer from diffusing into

the first layer. The portion in contact with the semiconductor layer is made of substantially stoichiometric titanium silicide. Thus, preferable ohmic contact can be derived.

[0015]

When a film of titanium silicide is formed, it is not necessary to intentionally add silicon. Titanium reacts with the silicon contained in the semiconductor layer. As a result, titanium silicide is automatically formed. For example, therefore, similar effects can be produced by depositing titanium containing less nitrogen onto the portion close to the semiconductor layer and depositing titanium containing more nitrogen onto the portion close to the second layer.

[0016]

In either case, in view of the whole first layer, it includes mainly of titanium and nitrogen. Preferably, the ratio of titanium to nitrogen (nitrogen/titanium) in the first layer is 0.5 to 1.2. This material containing titanium and nitrogen as a main component can make ohmic contact with a conductive oxide such as indium, tin oxide, zinc oxide, and nickel oxide. When aluminum and such the conductive oxide together form a junction, a thick layer of aluminum oxide is formed at this junction, and it is impossible to have good contact. In the prior art techniques, a chromium layer has been formed between aluminum and a conductive oxide. Since the chromium is poisonous, alternative materials have been sought for. Materials used in the present invention and including mainly of titanium and nitrogen are excellent also in this respect. Embodiment of the present invention is illustrated bellow and the structure of the invention is described in detail.

[0017]

[Example of the Invention]

[Example 1]

The present example is shown in FIGs. 1 and 2. FIG. 1 illustrates the procedure in which an electronic circuit having TFTs is manufactured. Description of conventional steps is omitted. First, an underlying silicon oxide film 2, an amorphous silicon film 3 with a thickness of 500 to 1500 Å, preferably 500 to 750 Å, and a protective layer 4 are formed over a glass substrate 1 made of Corning 7059 or the like. The laminate is annealed at 450 °C to 600 °C for 12 to 48 hours to crystallize the amorphous silicon film.

Needless to say, laser annealing or other similar means can be used for the crystallization (FIG. 1(A)).

[0018]

The silicon film is patterned into island-shaped semiconductor regions 5 and a silicon oxide film 6 with a thickness of 500 Å to 1500 Å; preferably 800 Å to 1000 Å are formed on the semiconductor regions 5 so as to form a gate oxide film. Then, gate wirings electrodes 7 are manufactured from aluminum. The aluminum wirings and electrodes 7 are anodized to form an aluminum oxide coating around the wirings and electrodes 7. This technique which makes use of anodization for top-gate TFTs in this way is described in Japanese Patent application Ser. No. 4-38637 (filed January 24, 1992). Needless to say, the gate electrodes can be made of silicon, titanium, tantalum, tungsten, molybdenum, or other material. Thereafter, using the gate electrodes as a mask, an impurity such as phosphorus is implanted by plasma doping or other method to form impurity regions (doped silicon regions) 8 aligned with the gate electrodes 7. Then, the impurity regions 8 are recrystallized by thermal annealing, laser annealing, or other method to form source and drain regions of TFTs (FIG. 1(B)).

[0019]

Then, an interlayer insulator (silicon oxide) 9 and conductive transparent oxide such as ITO (indium, tin oxide) are deposited. The ITO film is patterned into pixel electrodes 10 of an active-matrix liquid crystal display element. Contact holes are formed in the interlayer insulator 9 to expose a part of the impurity regions (source and drain regions). A first layer mainly including titanium and nitrogen is formed by sputtering. Also, a second layer made of aluminum is formed by sputtering in the manner described below.

[0020]

A target made of titanium is placed in a sputter chamber. Films are formed within argon ambient. The sputtering pressure is set to 1 to 10 mTorr. Then, a layer having titanium as its main component but containing little nitrogen is formed up to a thickness of 50 Å to 500 Å. Next, nitrogen is introduced into the sputter chamber besides argon. Within this ambient, a film is formed by sputtering. As a result, a layer of substantially stoichiometric titanium nitride with a thickness of 200 Å to 1000 Å is formed. At this time,

the percentage of nitrogen in the sputtering ambient is 40% or more. It is to be noted that the deposition rate by sputtering is affected greatly by the partial pressure of the nitrogen as well as by the sputtering pressure. For example, the deposition rate within ambient including only of argon is generally 3 to 5 times as high as the deposition rate within ambient containing 20% or more of nitrogen. With respect to the sputtering ambient, ammonia, hydradine, or other substance can be used instead of nitrogen. It is known that the resistivity of the produced film varies, depending on the partial pressure of nitrogen during sputtering. Since the film is used for a wiring material, a lower resistivity is desired. For this purpose, needless to say, an optimum partial pressure of nitrogen is adopted. For example, ambient containing 100% nitrogen produces a lower resistivity than the resistivity obtained within ambient containing 40% nitrogen. Typical resistivity is from 50 to 300 $\mu\Omega$cm.

[0021]

In the steps described above, when the titanium layer which is formed first and contains little nitrogen is too thick, reaction with the underlying semiconductor layer is occurred. And this made it impossible to obtain good contact. The result of the research of the present invention has demonstrated that it is preferable that titanium layer is thinner than the semiconductor layer.

[0022]

After forming a first layer 11 as described above, an aluminum (containing 1% silicon) film 12 is formed to have a thickness of 2000 Å to 5000 Å as a second layer by sputtering all in all. These layers are photolithographically patterned. More specifically, the second layer of aluminum is etched with an etchant such as a mixture acid of phosphoric acid, acetic acid, and nitric acid. Subsequently, the first layer is etched with buffered hydrofluoric acid or nitrous acid while leaving behind the resist on the aluminum film. At this time, careful attention is required since the interlayer insulator is deteriorated by overetching. The etching might also be carried out with a mixture of aqueous solution of hydrogen peroxide (H_2O_2) and aqueous ammonia (NH_3 OH), using the aluminum layer selectively left first as a mask. In this case, the interlayer insulator is not affected. However, careful attention is required since organic materials such as the photoresist are

oxidized.

[0023]

The above-described etching step can be a dry etching process. If carbon tetrachloride (CCl_4) is used as an etching gas, it is preferable that the second and first layers can be continuously etched without adversely affecting the silicon oxide. In this way, conductive wirings extending from the impurity regions are formed. Then, the laminate is annealed at 300 °C within ambient of hydrogen, thus completing TFTs.

[0024]

The circuit manufactured in this way has portions which require to be connected to the outside. FIG. 2(A) shows the manner in which conductive wirings 19 for connection with outside is formed from an integrated circuit 18 formed over the substrate 17 toward the peripheral portions of the substrate. This electronic circuit may sometimes make electrical contact by mechanical means such as contact fixtures (e.g., sockets) in regions 20 surrounded by the dotted line.

[0025]

In the liquid crystal display device shown in FIG. 2B, in order to supply electric power and signals to the circuits 22 to 24 for driving an active matrix region 25 over the substrate 21, electrical contact is made in regions 27 surrounded by the dotted lines. Connections made by wire bonding function permanently and are highly reliable. However, the method is not suited for connections of numerous terminals due to lots of trouble when manufacturing the wirings. Namely, use of mechanical contact may sometimes be more advantageous.

[0026]

In this case, however, it is necessary that the surfaces of the wiring at the contact be sufficiently strong and that the underlying layer adheres well to the wirings. Aluminum is not suitable for the purposes. A material including mainly of titanium adheres well to silicon, silicon oxide, aluminum, and other similar material. Also, the hardness of the coating of this material is high. Hence, this material is adequate. It is possible that nitrogen be not contained at all. Also, a maximum amount of nitrogen up to its stoichiometric ratio may be contained. In the present example, of the first layer 11, only

the contact is etched to expose the second layer. In the present example, the portions of the first layer 12 which are in contact with the second layer are made of stoichiometric titanium nitride. Contact fixtures 13 are pressed against the exposed portions of the titanium nitride to form contact (FIG. 1(C)).

[0027]

Alternatively, as shown in FIG. 1(D), a second layer 15 is formed on a first layer 14. A third layer 16 of titanium nitride is formed on the second layer 15. Contact fixture may be brought into contact with this third layer. In this case, it is not necessary to partially etch the second layer as shown in FIG.1(C). Hence, the patterning step can be omitted. Furthermore, as shown in FIG. 1(E), a layer including mainly of nitrogen and titanium according to the present invention is first patterned into wirings, and then an ITO film is formed. In either case, in the present example, the ITO film is made of a material mainly including nitrogen and titanium. Consequently, good contact can be obtained. The material of the film is not restricted to ITO. Rather, various other conductive oxides may also be used.

[0028]

The V_D -I_D characteristic of the TFTs obtained in this way is shown as a curve in FIG. 3. For reference, the V_D -I_D characteristic of TFTs having conventional Al/Si contact is shown as a curve b in FIG. 3. A kink is observed close to $V_D = 0$ on the curve b of the TFTs manufactured by the prior art method. Their contact resistances do not make ohmic contact. On the other hand, such abnormality is not observed on the curve of the TFTs manufactured according to the present invention, and normal MOSFET characteristics are exhibited.

[0029]

[Example 2]

The present example is described with reference to FIG. 1, which conceptually illustrates the procedure in which an electronic circuit having TFTs is manufactured. Conventional steps are not described herein. First, an underlying silicon oxide film 2, amorphous silicon film 3 with a film thickness of 100 Å to 1500 Å, preferably 100 Å to 750 Å, and protective layer 4 is deposited on a glass substrate 1 in procedure. The laminate is

annealed at 450 °C to 600 °C for 12 to 48 hours to crystallize the amorphous silicon. Of course, laser annealing or other similar means can be also used for the crystallization (FIG. 1(A)).

[0030]

The silicon film is patterned into an island-shaped semiconductor region 5. A silicon oxide film 6 having a thickness of 500 Å to 1500 Å, preferably 800 Å to 1000 Å, is formed on the semiconductor regions to form a gate oxide film. Then, gate wirings and electrodes 7 are formed from aluminum. The aluminum wirings and electrodes 7 are anodized to form an aluminum oxide coating around the wirings and electrodes 7. Thereafter, using the gate electrodes as a mask, an impurity such as phosphorus is introduced by ion implantation method or other method to form impurity regions (doped silicon regions) 8 aligned with the gate electrodes 7. The dose, the accelerating voltage, and the thickness of the gate oxide film are set so that the dose is 0.8 to $4\times10^{15}/cm^{-2}$ and that the impurity density is 1×10^{19} to $1\times10^{21}/cm^{-3}$. Then, the impurity regions 8 are recrystallized by thermal laser annealing, or other method to form source and drain regions of TFTs (FIG. 1(B)).

[0031]

Then, an interlayer insulator (silicon oxide) 9, and an ITO film are deposited. The ITO film is patterned so as to form a pixel electrode 10 of an active matrix type liquid crystal display element. Contact holes are formed in the interlayer insulator 9 to expose a part of the impurity regions (source and drain regions). A first layer mainly including titanium and nitrogen is formed by sputtering. Also, a second layer made of aluminum is formed by DC sputtering in the manner described below.

[0032]

A target made of titanium is placed in a sputter chamber. Films are formed within ambient including argon and nitrogen. The ratio of the partial pressure of the argon to the partial pressure of the nitrogen is 0.3 or less, for example films are formed within ambient where argon: nitrogen is 4:1. The sputtering pressure is 3 mTorr. A DC current of 4.5A is passed. The flow rate of the argon is 24 SCCM. The flow rate of the nitrogen is 6 SCCM. A lower layer of the first layer containing less nitrogen is formed with a thickness

of 100 Å. The film formed in this way showed sufficiently small contact resistance with the silicon and ITO.

[0033]

Then, the nitrogen percentage of the ambient within the sputter chamber is increased such that the ratio of the partial pressure of the argon to the partial pressure of the nitrogen is 0.3 or more, for example 1:1. Within this ambient, a film is formed by sputtering. The sputtering pressure and the DC current are maintained at 3 mTorr and 4.5A, respectively. The flow rates of the argon and the nitrogen are set to 15 SCCM. By the steps described above, an upper layer of the first layer is formed with a thickness of 900 Å. The film formed in this manner has a large contact resistance with the silicon and so not able to be used as contact. However, this film could be patterned into wirings without difficulty in the present example. It is to be noted that the deposition rate by sputtering is affected greatly by the partial pressure of the nitrogen as well as by the sputtering pressure. For example, where the ratio of argon to nitrogen is 4:1, the deposition rate is 100 Å to 120 Å/min. Where the ratio of argon to nitrogen is 1:1, the deposition rate is 30 Å to 40 Å/min.

[0034]

After forming the first layer 11 in this way, aluminum is sputtered to form a second layer 12 containing 1% silicon with a thickness of 2000 Å to 5000 Å. These layers are photolithographically patterned. More specifically, the second layer of aluminum is etched with an etchant such as a mixture acid of phosphoric acid, acetic acid, and nitric acid. Subsequently, the first layer is etched with a mixture liquid of aqueous solution of hydrogen peroxide (H_2O_2) and aqueous ammonia (NH_3) while leaving behind the photo resist on the aluminum film. Since this etchant oxidizes organic substances, it follows that a final cleaning of organic substances is simultaneously done. In this way, after wirings extending from the impurity regions are formed, the laminate is annealed at 300 °C within ambient of hydrogen, thus completing TFTs. In the present example of the first layer 12, only the contact is etched, thus exposing the second layer. Contact fixtures 13 are pressed against the exposed portions of the first layer to form contact (FIG. 1(C)).

[Effect of the Invention]

According to the present invention, preferable contact can be formed in a thin source, drain, or impurity region, of TFTs. The contact has a higher reliability, thus being effective in enhancing the reliability of the whole electronic circuit. Accordingly, the present invention is industrially advantageous.

[Brief Description Of the Drawings]

FIG. 1 shows an example (cross sectional view) of a circuit having a TFT according to the present invention.

FIG. 2 shows an example (top view) of an electronic circuit according to the present invention.

FIG. 3 shows a characteristic (a) of a TFT obtained by the examples and a characteristic (b) of a TFT obtained by the prior art.

[Description of symbol]

1. glass substrate
2. underlying silicon oxide layer
3. silicon film
4. protective film
5. island-shaped semiconductor region
6. silicon oxide film (gate oxide film)
7. gate electrode/ wiring (aluminum covered with anode oxide film)
8. impurity region
9. interlayer insulator (silicon oxide)
10. pixel electrode (ITO)
11. first layer (titanium nitride)
12. second layer (aluminum)
13. contact fixtures
14. first layer (titanium nitride)
15. second layer (aluminum)
16. third layer (titanium nitride)

[Document Name] Abstract of the Disclosure

[Summary]

[Object of the Invention]

Preferable contact is to be formed between a metal wiring and a semiconductor layer. And reliability of en electronic circuit is to be improved.

[Structure]

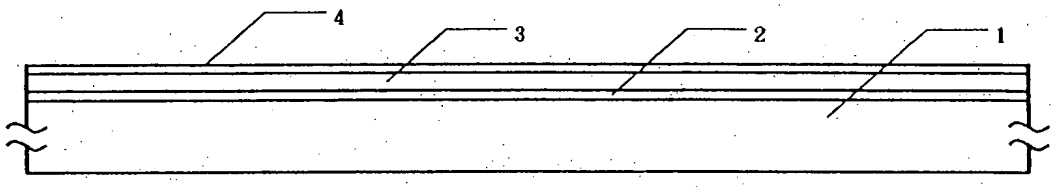
An electronic circuit having a semiconductor film mainly including silicon with a thin thickness over an insulating substrate, comprising a first layer including titanium and nitrogen as a main material as adhering to the semiconductor film, and a wiring formed from a second layer including aluminum as a main component as adhering to the first layer.

[Selected drawing] FIG. 1

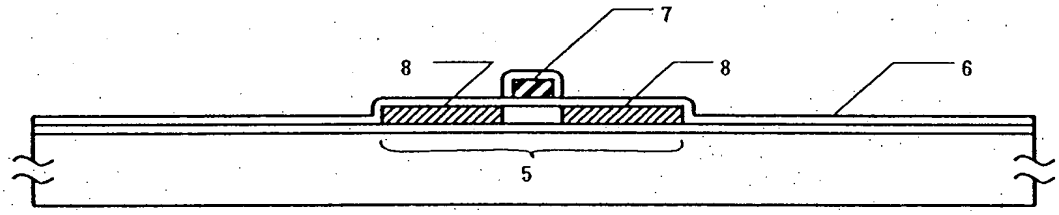
[Reference Number] P002252-04

[Name of Document] Drawing

FIG. 1



(A)



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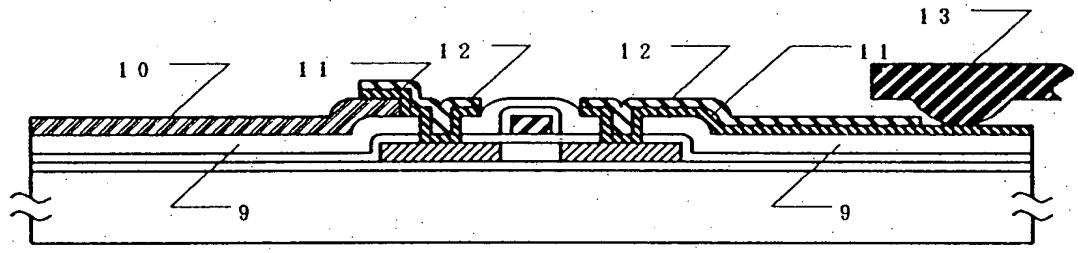

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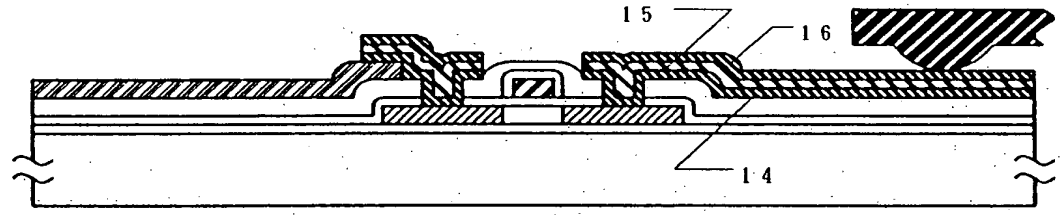
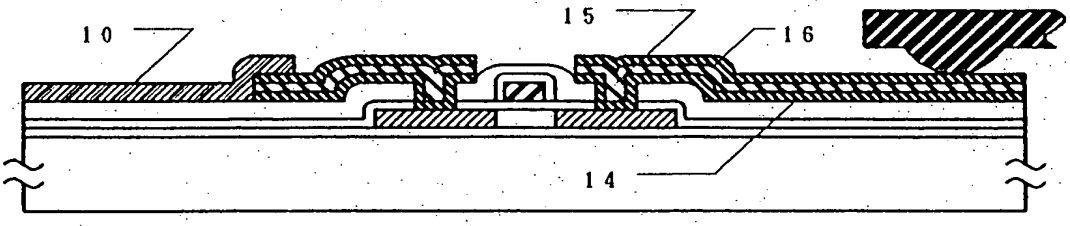


(D)



(E)

aluminum (gate electrode·wiring)

TiN.

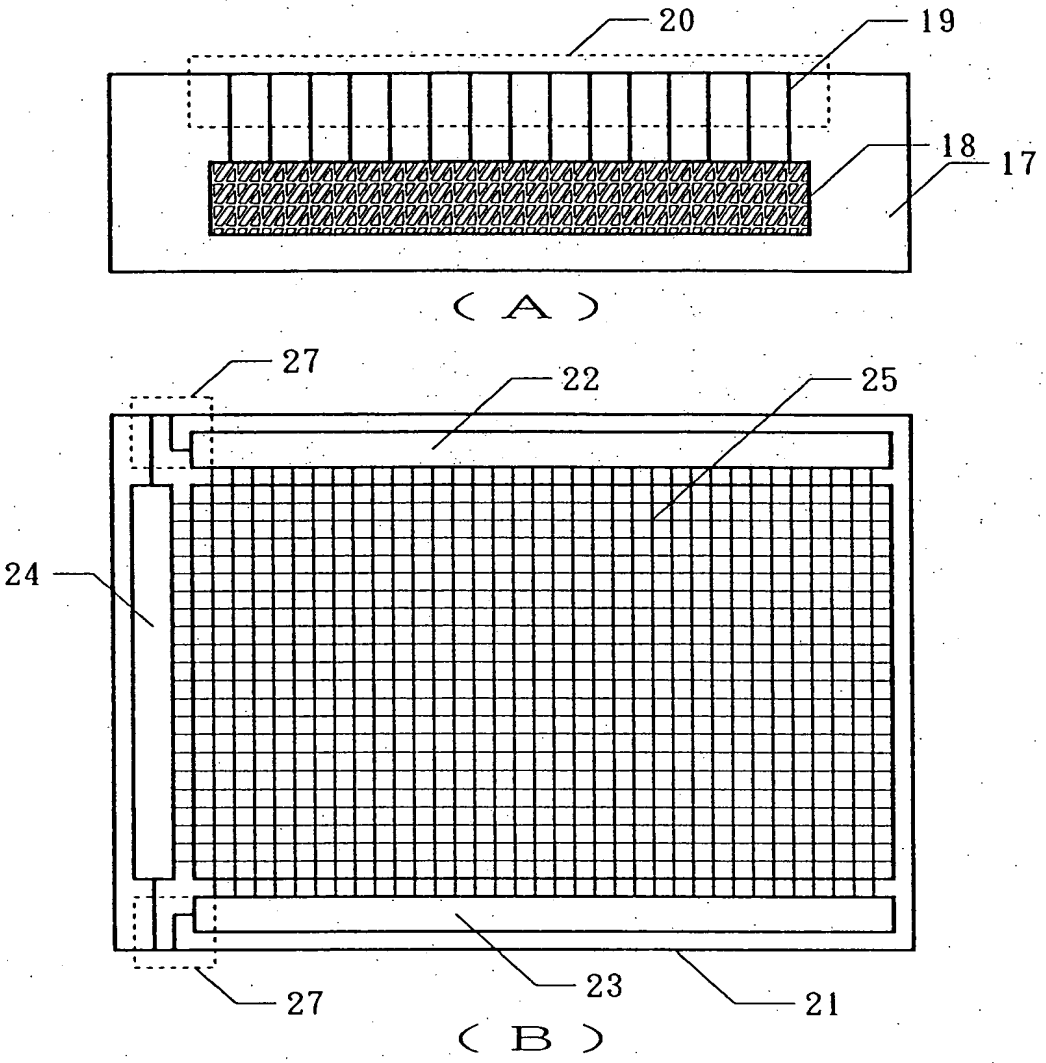
doped silicon (source, drain)

aluminum (second layer wiring)

ITO (pixel electrode)

[Reference Number] P002252-04

FIG. 2



[Reference Number] P002252-04

FIG. 3